DOCKET NO. 00-BN-059 (STMI01-00059) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

The undersigned hereby certifies that the following documents:

1. Appeal Brief;
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3. Check in the amount of $500.00 (for the Appeal Brief filing fee); and
4. A postcard receipt

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to MAIL STOP **APPEAL BRIEF-PATENTS**, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 24, 2006.

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FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/751,674
Filing Date	December 29, 2000
First Named Inventor	Paolo Faraboschi
Examiner Name	Aimee J. Li
Art Unit	2183
Attorney Docket No.	00-BN-059 (STMI01-00059)

METHOD OF PAYMENT (check all that apply)

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☑ Deposit Account Deposit Account Number: 50-0208 Deposit Account Name: Davis Munck P.C.

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____	/ 50 = _____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Appeal Brief fee	$500.00

SUBMITTED BY

Signature	William A. Munck	Registration No. (Attorney/Agent) 39,308	Telephone (972) 628-3600
Name (Print/Type)	William A. Munck		Date April 24, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Serial No.:	09/751,674
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Examiner:	Aimee J. Li

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APPEAL BRIEF

Sir:

Applicants herewith respectfully submit that the Examiner's decision of October 7, 2005, finally rejecting Claims 1-22 in the present application, should be reversed, in view of the following arguments and authorities. This Brief is submitted on behalf of Appellant for the application identified above. A check is enclosed for the fee for filing a Brief on Appeal. Please charge any additional necessary fees to Deposit Account No. 50-0208.

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TABLE OF CONTENTS

APPENDIX B - Copy of Formal Drawings

APPENDIX C - Evidence Appendix.- No additional evidence was submitted.

APPENDIX D - Related Proceedings Appendix - There are no related proceedings.

TABLE OF AUTHORITIES

Real Party in Interest

The real party in interest, and assignee of this case, is STMicroelectronics, Inc..

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

Status of Claims

Claims 1-22 are under final rejection, and are each appealed.

Status of Amendments after Final

No amendments to the claims were made after final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

In General

The present application is directed, in general, to an apparatus for compressing and dispersing instructions a wide-issue data processor, and related methods and systems. *Page 2, lines 5-7, and Figures 1 - 8.*

Support for Independent Claims

Note that, per 37 CFR §41.37, only each of the independent claims are discussed in this section. In the arguments below, however, the dependent claims are also discussed and distinguished from the prior art. The discussion of the claims is for illustrative purposes, and is not intended to effect the scope of the claims.

Independent Claim 1 describes a data processor 100 including a plurality of execution clusters 220-222, each of the execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables A0/A1, wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles. *Page 12, lines 2-12; and Figure 2, reproduced next page.*

Independent Claim 1 also describes that data processor 100 includes an instruction cache 215 capable of storing a plurality of cache lines, each of said cache lines comprising a plurality of the syllables. *Page 12, lines 12-14; and Figure 2.*

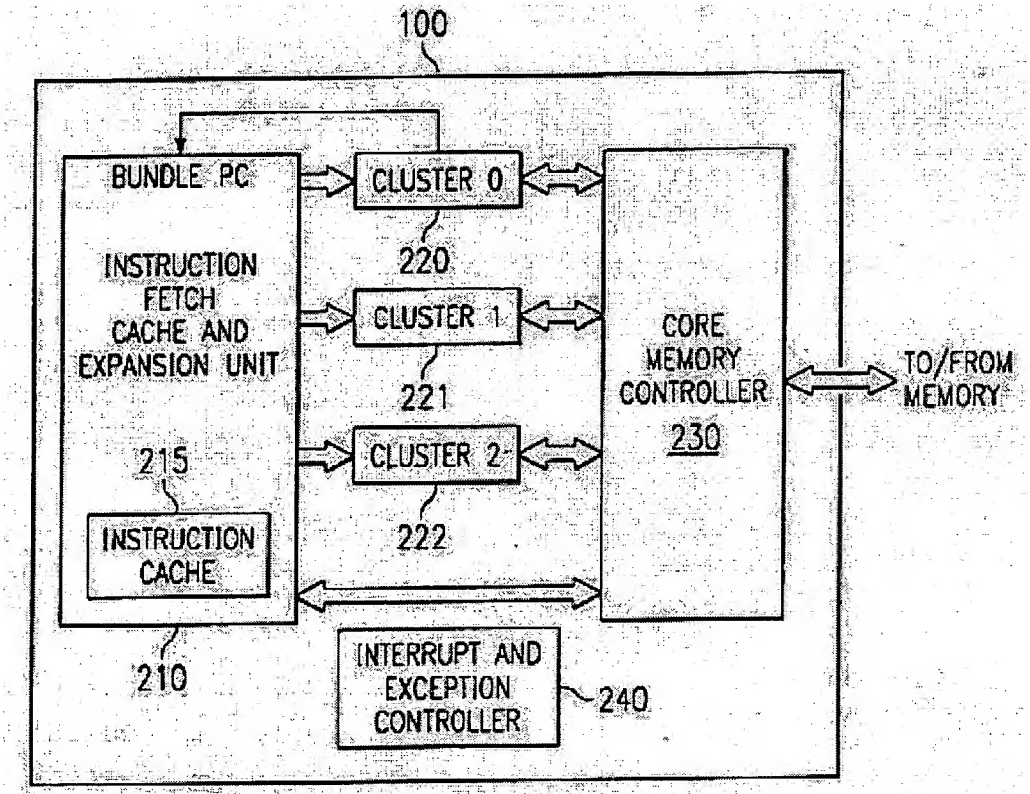

FIG. 2

Independent Claim 1 also describes that data processor 100 includes an instruction issue unit 500 capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment. Page 12, lines 14-16; page 40, line 5; page 31, line 22 - page 32, line 12; page 39, line 17 - page; and Figure 5, reproduced at right.

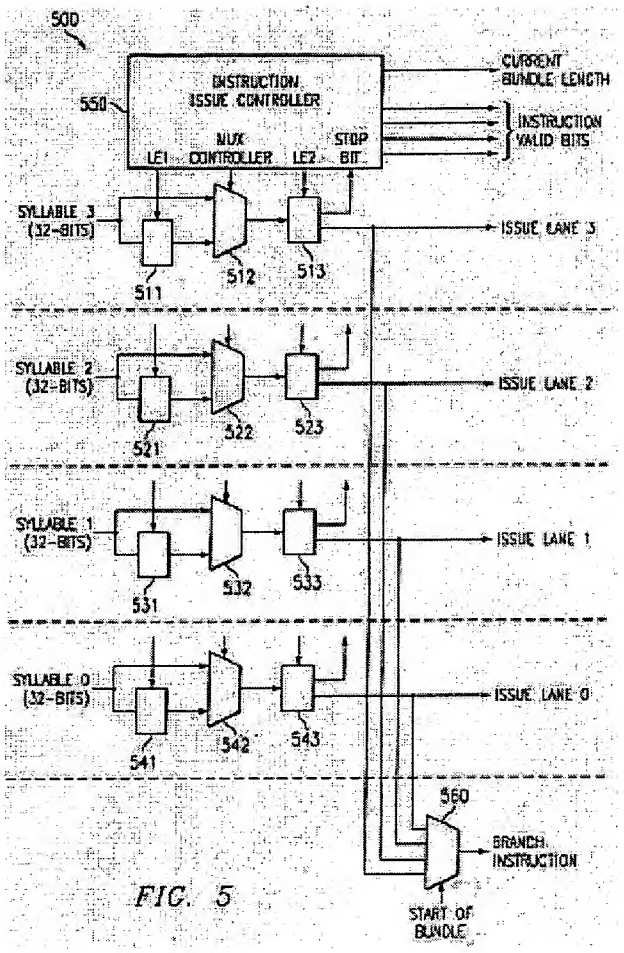

FIG. 5

Independent Claim 1 also describes that data processor 100 includes alignment and dispersal circuitry 810 capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles, the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes. *Page 12, line 17 - page 13, line 1; page 40, line 5; page 31, line 22 - page 32, line 12; page 39, line 17 - page; page 42, lines 8-16; and Figure 8, reproduced next page.*

Independent Claim 10 describes a processing system 10 comprising a data processor 100; a memory 140/150 coupled to said data processor; and a plurality of memory-mapped peripheral circuits 111-114 coupled to said data processor for performing selected functions in association with said data processor. Independent Claim 1 describes that the data processor 100 comprises a plurality of execution clusters 220-222, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables A0/A1, wherein each of said instruction execution pipelines is a

plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles; an instruction cache 215 capable of storing a plurality of cache lines, each of said cache lines comprising a plurality of the syllables; an instruction issue unit 500 capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment; and alignment and dispersal circuitry 810 capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles, the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes. *Page 12, line 2 - page 13, line 1; page 40, line 5; page 31, line 22 - page 32, line 12; page 39, line 17 - page; page 42, lines 8-16; and Figures 1, 2, 5, and 8.*

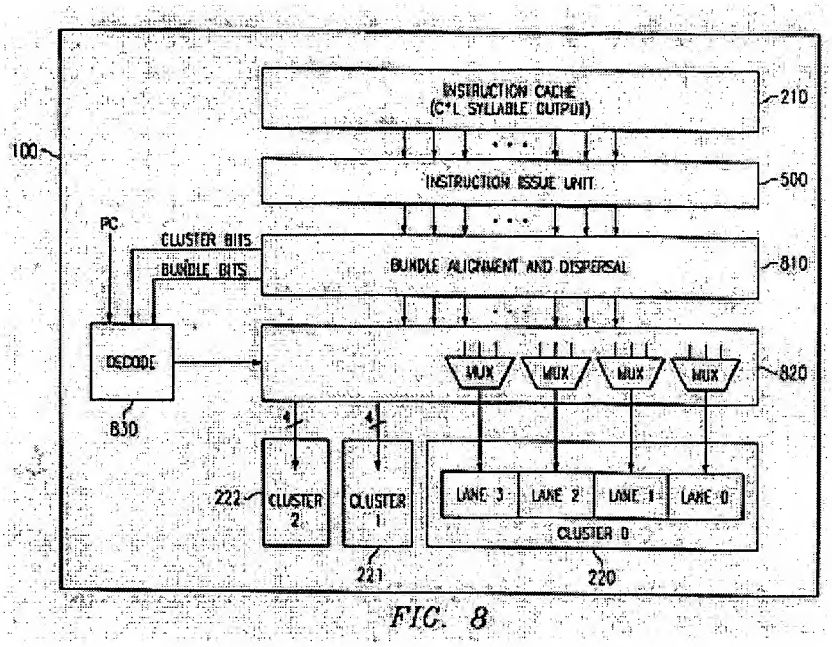

FIG. 8

Independent Claim 19 describes, for use in a data processor 100 comprising a plurality of execution clusters 220-222, each of the execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables A0/A1, wherein each of the instruction execution pipelines is a plurality of lanes wide, each of the lanes capable of receiving one or more of the syllables of the instruction bundles, a method of routing instruction bundles into the lanes in the execution clusters comprising the steps of fetching cache lines from an instruction cache 215, each of the cache lines comprising a plurality of the syllables; issuing complete instruction bundles toward the execution

clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment; reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes; and routing each of the complete instruction bundles to a correct one of the execution clusters as a function of at least one of: 1) at least one address bit associated with each of the complete instruction bundles; 2) at least one address bit associated with at least one syllable in each of the complete instruction bundles; and 3) a cluster bit associated with each of the complete instruction bundles. *Page 12, line 2 - page 13, line 1; page 40, line 5; page 31, line 22 - page 32, line 12; page 39, line 17 - page; page 42, lines 8-16; and Figures 1, 2, 5, and 8.*

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-22 obvious over U.S. Patent No. 5,819,058 to Miller *et al.* ("Miller") in view of U.S. Patent No. 6,167,503 to Jouppi ("Jouppi")?

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

In Section 2 of the October 7, 2005 Office Action, Claims 1-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,819,058 to Miller *et al.* ("Miller") in view of U.S. Patent No. 6,167,503 to Jouppi ("Jouppi").

Legal Standards

The legal standards for an obviousness[1] rejection are referenced in the footnote below.

Analysis of Examiner's Rejection

The cited references are each briefly discussed in relevant part, and then the rejection of each claim is addressed separately under each ground of rejection.

Miller, the primary reference used in the final Office Action, is drawn to an instruction compression and decompression system and method that uses variable-length instruction packets in a processor having a plurality of processing units . While Miller shares some structural similarities with the instant application, it does not include several claimed elements and functions, as described in detail below, and as conceded by Examiner Li.

Jouppi is drawn to a register and instruction controller for a superscalar processor. Jouppi dies includes a plurality of clusters for executing the instructions. As such, Jouppi does address

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[1]The Supreme Court has explained how to apply §103:

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined.
>
> *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459, 467 (1966).

Obviousness cannot be inferred from a combination of references without a showing that one of ordinary skill would have been motivated to combine those references:

> When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.
>
> *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 U.S.P.Q.2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 U.S.P.Q. 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 U.S.P.Q. 481 (Fed.Cir. 1984).

some issues similar to those of the present application, but not in the manner contemplated by the claims, as described in detail below.

Ground of Rejection 1: Claims 1-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,819,058 to Miller et al. ("Miller") in view of U.S. Patent No. 6,167,503 to Jouppi ("Jouppi").

Claim 1

A data processor comprising:

a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages 305/310/625 capable of executing instruction bundles each comprising one or more syllables, wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising a plurality of the syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment; and

alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles, the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes.

Claim 1 therefore requires an "instruction issue unit" that issues "complete instruction bundles" toward multiple execution clusters, where at least one complete instruction bundle is "issued having an out-of-order alignment." Claim 1 also requires "alignment and dispersal circuitry" capable of "reordering each of the at least one complete instruction bundle having the out-of-order alignment" so as to "align the syllables in the complete instruction bundle with correct ones of the lanes."

While this appeal is necessarily directed to the final Office Action, in the subsequent Advisory Action, Examiner Li for the first time alleged that Miller's "decompressor" 178 functions as the claimed "instruction issue unit". Examiner Li's allegation is in error.

Claim 1 requires that the instruction issue unit be capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward the execution clusters, where at least one complete instruction bundle is issued having an out-of-order alignment.

Examiner Li indicated that this is satisfied by Miller's decompressor 178, which receives compressed instructions, uncompresses them, and puts the resulting very long instruction word 292 into a very long instruction register 180. Various bits of the register 180, forming specific instructions, are then read by an execution control unit (ECU) 26, multiplier unit (MUL) 30, an arithmetic logic unit (ALU) 32, register control unit (RCU) 34, and memory unit (MEM) 36, which Miller considers each to be a "processing unit".

Even assuming (without conceding) that Miller's very long instruction word 292 corresponds to the claimed "complete instruction bundle", nothing in Miller teaches or suggests that at least one complete instruction bundle is issued having an out-of-order alignment. Examiner Li makes reference to Miller's discussion of "default instructions" in col. 9-10, where Miller describes that default instructions can be inserted where the end of a compressed packet is detected. Here, nothing indicates that any of the actual instruction are out of order - using default instructions for a processor that has no compressed instruction does not imply that the actual instructions for other processors are therefore out-of-order, and Miller makes no teaching or suggestion that this is the case.

Claim 1 also requires alignment and dispersal circuitry capable of receiving said complete instruction bundles from the instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles. The Examiner alleges that Miller's multiplexers 224, 226, 228, 230, 232 satisfy this element. However, claim 1 also requires that the

alignment and dispersal circuitry be also capable of reordering the complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes. Nothing in Miller teaches or suggests that multiplexers 224, 226, 228, 230, 232 are capable of re-ordering the bits or syllables they receive when producing the very long instruction word 292, nor that the very long instruction register 180 can do so.

Note that Examiner Li at no point has specifically identified where this feature is taught by Miller, and certainly has not shown where this function is taught to be performed by multiplexers 224, 226, 228, 230, 232. Miller does not teach or suggest anything related to reordering instruction bundles to accommodate our-of-order instruction bundles. By failing to show where this feature of claim 1 is taught or suggested by the art of record, Examiner Li has failed to make even a prima facie obviousness rejection.

Examiner Li concedes that Miller teaches nothing like the claimed execution clusters, and refers to Jouppi. Jouppi discusses parallel execution clusters in a superscalar computer system. Evidently, Examiner Liu believes that one of skill in the art would be motivated to insert a superscalar computer system execution unit in place of each of the execution control unit, multiplier unit, an arithmetic logic unit, register control unit, and memory unit of Miller's processor, and that to do so would be more efficient and would not increase circuit complexity.

Claim 1 requires that the complete instruction bundles be issued toward a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, and wherein each of said instruction execution pipelines is a plurality of lanes

wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles.

Even if Miller and Jouppi could somehow be combined, other than a discussing execution clusters, Jouppi has little in common with the claimed invention. For example, Jouppi lacks any teaching or suggestion that particular instructions must be executed by particular lanes in the computer system, as required by claim 1. Further, Jouppi lacks any mention that particular instructions must be executed by particular ones of the execution units 250, 251 in the execution clusters 280, 290. Instead, Jouppi simply recites that instructions are provided to multiple execution units, which execute the instructions in parallel.

Because of this, Jouppi fails to teach or suggest an "instruction issue unit" that issues "complete instruction bundles" toward multiple execution clusters, where at least one complete instruction bundle is "issued having an out-of-order alignment" as recited in Claim 1. Jouppi also fails to teach or suggest "alignment and dispersal circuitry" capable of "reordering each of the at least one complete instruction bundle having the out-of-order alignment" so as to "align the syllables in the complete instruction bundle with correct ones of the lanes" as recited in Claim 1.

For these reasons, Jouppi also fails to teach or suggest the Applicants' invention as recited in Claim 1 (and its dependent claims).

Further, even if all limitations of independent Claim 1 were taught by Miller, Jouppi, or some combination of these, there is no proper motivation to combine these references, as addressed in more detail below.

Therefore, Examiner Li's final Office Action fails to establish that the proposed Miller-Jouppi combination discloses, teaches, or suggests all elements of Claim 1. The rejection of this

claim, and all its dependent claims, should be reversed, and these claims should be allowed over all art of record.

Claim 2

Claim 2 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles".

As Claim 2 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or the at least one address bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 3

Claim 3 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles".

As Claim 3 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment

and dispersal circuitry or the at least one cluster bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 4

Claim 4 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles".

As Claim 4 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or the at least one cluster bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 5

Claim 5 requires, among other limitations, that the "said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said execution clusters".

As Claim 5 depends from claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference, in particular because no reference includes the claimed alignment and dispersal circuitry.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 6

Claim 6 requires, among other limitations, that the "alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry."

As Claim 6 depends from claim 5, the arguments above with regard to Claims 1 and 5 apply here as well, and are incorporated herein by reference, in particular because no reference includes the claimed alignment and dispersal circuitry.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 7

Claim 7 requires, among other limitations, that the said control logic circuitry controls said multiplexer circuitry as a function of at least one of: 1) said at least one address bit associated with each of said complete instruction bundles; 2) at least one address bit associated with at least one syllable in each of said complete instruction bundles; and 3) a cluster bit associated with each of said complete instruction bundles".

As Claim 7 depends from Claim 6, the arguments above with regard to Claims 1, 5, and 6 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or a bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 8

Claim 8 requires, among other limitations, that "each execution pipeline is four lanes wide".

As Claim 8 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 9

Claim 9 requires, among other limitations, that the data processor comprises three execution units".

As Claim 9 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 10

Claim 10 requires an "instruction issue unit" that issues "complete instruction bundles" toward multiple execution clusters, where at least one complete instruction bundle is "issued having an out-of-order alignment." Claim 10 also requires "alignment and dispersal circuitry" capable of "reordering each of the at least one complete instruction bundle having the out-of-order alignment" so as to "align the syllables in the complete instruction bundle with correct ones of the lanes."

Examiner Li alleged in the Advisory Action that Miller's "decompressor" 178 functions as the claimed "instruction issue unit". Examiner Li's allegation is in error.

Claim 10 requires that the instruction issue unit be capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward the execution clusters, where at least one complete instruction bundle is issued having an out-of-order alignment.

Examiner Li indicated that this is satisfied by Miller's decompressor 178, which receives compressed instructions, uncompresses them, and puts the resulting very long instruction word 292

into a very long instruction register 180. Various bits of the register 180, forming specific instructions, are then read by an execution control unit (ECU) 26, multiplier unit (MUL) 30, an arithmetic logic unit (ALU) 32, register control unit (RCU) 34, and memory unit (MEM) 36, which Miller considers each to be a "processing unit".

Even assuming (without conceding) that Miller's very long instruction word 292 corresponds to the claimed "complete instruction bundle", nothing in Miller teaches or suggests that at least one complete instruction bundle is issued having an out-of-order alignment. Examiner Li makes reference to Miller's discussion of "default instructions" in col. 9-10, where Miller describes that default instructions can be inserted where the end of a compressed packet is detected. Here, nothing indicates that any of the actual instruction are out of order - using default instructions for a processor that has no compressed instruction does not imply that the actual instructions for other processors are therefore out-of-order, and Miller makes no teaching or suggestion that this is the case.

Claim 10 also requires alignment and dispersal circuitry capable of receiving said complete instruction bundles from the instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles. Examiner Li alleges that Miller's multiplexers 224, 226, 228, 230, 232 satisfy this element. However, claim 10 also requires that the alignment and dispersal circuitry be also capable of reordering the complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes. Nothing in Miller teaches or suggests that multiplexers 224, 226, 228, 230, 232 are capable of re-ordering the bits or syllables they receive when producing the very long instruction word 292, nor that the very long instruction register 180 can do so.

Note that Examiner Li at no point has specifically identified where this feature is taught by Miller, and certainly has not shown where this function is taught to be performed by multiplexers 224, 226, 228, 230, 232. Miller does not teach or suggest anything related to reordering instruction bundles to accommodate our-of-order instruction bundles. By failing to show where this feature of claim 10 is taught or suggested by the art of record, Examiner Li has failed to make even a prima facie obviousness rejection.

Examiner Li concedes that Miller teaches nothing like the claimed execution clusters, and refers to Jouppi. Jouppi discusses parallel execution clusters in a superscalar computer system. Evidently, Examiner Liu believes that one of skill in the art would be motivated to insert a superscalar computer system execution unit in place of each of the execution control unit, multiplier unit, an arithmetic logic unit, register control unit, and memory unit of Miller's processor, and that to do so would be more efficient and would not increase circuit complexity.

Claim 10 requires that the complete instruction bundles be issued toward a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, and wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles.

Even if Miller and Jouppi could somehow be combined, other than a discussing execution clusters, Jouppi has little in common with the claimed invention. For example, Jouppi lacks any teaching or suggestion that particular instructions must be executed by particular lanes in the computer system, as required by claim 10. Further, Jouppi lacks any mention that particular

instructions must be executed by particular ones of the execution units 250, 251 in the execution clusters 280, 290. Instead, Jouppi simply recites that instructions are provided to multiple execution units, which execute the instructions in parallel.

Because of this, Jouppi fails to teach or suggest an "instruction issue unit" that issues "complete instruction bundles" toward multiple execution clusters, where at least one complete instruction bundle is "issued having an out-of-order alignment" as recited in Claim 10. Jouppi also fails to teach or suggest "alignment and dispersal circuitry" capable of "reordering each of the at least one complete instruction bundle having the out-of-order alignment" so as to "align the syllables in the complete instruction bundle with correct ones of the lanes" as recited in Claim 10.

For these reasons, Jouppi also fails to teach or suggest the Applicants' invention as recited in Claim 10 (and its dependent claims).

Further, even if all limitations of independent Claim 10 were taught by Miller, Jouppi, or some combination of these, there is no proper motivation to combine these references, as addressed in more detail below.

Therefore, Examiner Li's final Office Action fails to establish that the proposed Miller-Jouppi combination discloses, teaches, or suggests all elements of Claim 10. The rejection of this claim, and all its dependent claims, should be reversed, and these claims should be allowed over all art of record.

Claim 11

Claim 11 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at

least one address bit associated with at least one syllable in each of said complete instruction bundles".

As Claim 11 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or the at least one address bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 12

Claim 12 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles".

As Claim 12 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or the at least one cluster bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 13

Claim 13 requires, among other limitations, "alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles".

As Claim 13 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or the at least one cluster bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 14

Claim 14 requires, among other limitations, that the "said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said execution clusters".

As Claim 14 depends from claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference, in particular because no reference includes the claimed alignment and dispersal circuitry.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 15

Claim 15 requires, among other limitations, that the "alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry."

As Claim 15 depends from claim 14, the arguments above with regard to Claims 10 and 14 apply here as well, and are incorporated herein by reference, in particular because no reference includes the claimed alignment and dispersal circuitry.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 16

Claim 16 requires, among other limitations, that the said control logic circuitry controls said multiplexer circuitry as a function of at least one of: 1) said at least one address bit associated with each of said complete instruction bundles; 2) at least one address bit associated with at least one syllable in each of said complete instruction bundles; and 3) a cluster bit associated with each of said complete instruction bundles".

As Claim 16 depends from Claim 15, the arguments above with regard to Claims 10, 14, and 15 apply here as well, and are incorporated herein by reference. Nothing in Miller or Jouppi teaches a alignment and dispersal circuitry or a bit that functions as claimed. Examiner Li has not, and cannot, identify this teaching in the art of reference.

Nothing in Miller, Jouppi, or any combination of them teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 17

Claim 17 requires, among other limitations, that "each execution pipeline is four lanes wide".

As Claim 17 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 18

Claim 18 requires, among other limitations, that the data processor comprises three execution units".

As Claim 18 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference.

Nothing in Miller teaches or suggests this particular circuit arrangement with regard to the required functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 19

Claim 10 requires, among other limitations,

> issuing complete instruction bundles toward the execution clusters,
>
> wherein at least one complete instruction bundle is issued having an out-of-order alignment;
>
> reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes; and
>
> routing each of the complete instruction bundles to a correct one of the execution clusters....

Examiner Li does not specifically identify where Miller or Jouppi allegedly perform these claimed steps, instead referring to large portions of their disclosures as a whole.

Claim 19 requires issuing complete instruction bundles toward the execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment.

Even assuming (without conceding) that Miller's very long instruction word 292 corresponds to the claimed "complete instruction bundle", nothing in Miller teaches or suggests that at least one complete instruction bundle is issued having an out-of-order alignment. Nothing in Miller indicates that any of the actual instruction are out of order - using default instructions for a processor that has no compressed instruction does not imply that the actual instructions for other processors are therefore out-of-order, and Miller makes no teaching or suggestion that this is the case.

Claim 19 also requires reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct

ones of the lanes. Nothing in Miller teaches or suggests that any element, including multiplexers 224, 226, 228, 230, 232, are capable of re-ordering the bits or syllables they receive when producing the very long instruction word 292, nor that the very long instruction register 180 can do so.

Note that Examiner Li at no point has specifically identified where this feature is taught by Miller, and certainly has not shown where this function is taught to be performed by multiplexers 224, 226, 228, 230, 232. Miller does not teach or suggest anything related to reordering instruction bundles to accommodate our-of-order instruction bundles. By failing to show where this feature of claim 19 is taught or suggested by the art of record, Examiner Li has failed to make even a prima facie obviousness rejection.

Examiner Li concedes that Miller teaches nothing like the claimed execution clusters, and refers to Jouppi. Jouppi discusses parallel execution clusters in a superscalar computer system. Evidently, Examiner Liu believes that one of skill in the art would be motivated to insert a superscalar computer system execution unit in place of each of the execution control unit, multiplier unit, an arithmetic logic unit, register control unit, and memory unit of Miller's processor, and that to do so would be more efficient and would not increase circuit complexity.

Claim 19 requires issuing complete instruction bundles toward the execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment, and after reordering, routing each of the complete instruction bundles to a correct one of the execution clusters.

Even if Miller and Jouppi could somehow be combined, other than a discussing execution clusters, Jouppi has little in common with the claimed invention. For example, Jouppi lacks any teaching or suggestion that particular instructions must be executed by particular lanes in the

computer system, as required by claim 19. Further, Jouppi lacks any mention that particular instructions must be executed by particular ones of the execution units 250, 251 in the execution clusters 280, 290. Instead, Jouppi simply recites that instructions are provided to multiple execution units, which execute the instructions in parallel.

For these reasons, Jouppi also fails to teach or suggest the Applicants' invention as recited in Claim 19 (and its dependent claims).

Further, even if all limitations of independent Claim 19 were taught by Miller, Jouppi, or some combination of these, there is no proper motivation to combine these references, as addressed in more detail below.

Therefore, Examiner Li's final Office Action fails to establish that the proposed Miller-Jouppi combination discloses, teaches, or suggests all elements of Claim 19. The rejection of this claim, and all its dependent claims, should be reversed, and these claims should be allowed over all art of record.

Claim 20

Claim 20 requires, among other limitations, that "each execution pipeline is four lanes wide and the data processor comprises three execution units."

As Claim 20 depends from Claim 19, the arguments above with regard to Claim 19 apply here as well, and are incorporated herein by reference.

Nothing in Miller or Jouppi teaches or suggests this particular circuit arrangement with regard to the method recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 21

Claim 21 requires, among other limitations, that "each of the execution clusters comprises one or more arithmetic units, a register file, an interface to a memory controller, and an inter-cluster communication interface."

As Claim 21 depends from Claim 1, the arguments above with regard to Claim 1 apply here as well, and are incorporated herein by reference.

Nothing in Miller or Jouppi teaches or suggests this particular circuit arrangement with regard to the limitations and functionality recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Claim 22

Claim 22 requires, among other limitations, that "each of the execution clusters comprises one or more arithmetic units, a register file, an interface to a memory controller, and an inter-cluster communication interface."

As Claim 22 depends from Claim 10, the arguments above with regard to Claim 10 apply here as well, and are incorporated herein by reference.

Nothing in Miller or Jouppi teaches or suggests this particular circuit arrangement with regard to the system recited in the parent claim. The rejection of this claim should be reversed, and it should be allowed over all art of record.

Therefore, all claims should be allowed over the combination of Miller and Jouppi, and Examiner Li's obviousness rejections should be reversed.

Motivation to Combine or Modify[2]

Examiner Li makes a variety of statements as alleged "motivations" to combine the Miller and Jouppi references, but these "motivations" are not taught or suggested by the art of record.

Evidently, Examiner Liu believes that one of skill in the art would be motivated to insert a superscalar computer system execution unit in place of each of the execution control unit, multiplier unit, an arithmetic logic unit, register control unit, and memory unit of Miller's processor, and that to do so would be more efficient and would not increase circuit complexity. The Examiner's

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[2]Where an obviousness rejection is based on a combination of references, the Examiner must show that one of ordinary skill would have been motivated to combine those references. *See In re Nilssen*, 7 USPQ2d 1500 (Fed.Cir. 1988); *Panduit Corp. v. Dennison Mfg. Co.*, 1 USPQ2d 1593, 1597 (Fed.Cir. 1987); *ACS Hospital Systems v. Montefiore Hospital*, 220 USPQ 929 (Fed.Cir. 1984).

"When prior art references require selective combination ... to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself.... Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination." *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 5 USPQ2d 1434, 1438 (Fed.Cir. 1988), *quoting Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed.Cir. 1985), *and Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick*, 221 USPQ 481 (Fed.Cir. 1984).

"While *[a reference]* may be capable of being modified to run the way *[the applicant's]* apparatus is Claimed, there must be a suggestion or motivation in the reference to do so. See In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) ("The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."). *In re Mills,* 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed.Cir. 1990).

conclusion is believed to be factually and logically erroneous, and the combination of references therefore both unmotivated and potentially inoperable.

As Examiner Li should be aware, the motivation to combine or modify must be specific to the actual teachings sought to be combined. "In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." (*Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1385 (Fed. Cir. 2001) emphasis added). "When the references are in the same field as that of the applicant's invention, knowledge thereof is presumed. However, the test of whether it would have been obvious to select specific teachings and combine them as did the applicant must still be met by identification of some suggestion, teaching, or motivation in the prior art, arising from what the prior art would have taught a person of ordinary skill in the field of the invention." (*In re Dance*, 160 F.3d 1339, 1343 (Fed. Cir. 1998), emphasis added).

Examiner Li has made no showing at all of a specific motivation to combine Miller and Jouppi in such a ways as to produce the claimed invention. As such, all rejections should be reversed for lack of motivated combination.

Grouping of Claims

The claims on appeal do not stand or fall together, as may be seen from the arguments set forth below. Each claim has been argued separately under a separate subheading, and each claim should be considered separately. While the applicant recognizes that a formal statement regarding the grouping of claims is no longer required, each claim should be considered separately; or at the very least each claim which is argued separately in the preceding sections of this brief should be considered separately. Argument: The fact that the claims use different formulations (as detailed above) and/or have been argued separately, shows that, if their patentability is not considered separately, any adverse decision would show that the limitations of some claims had been unfairly ignored.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,

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Date: April 24, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX A -

Claims Appendix

1. (Previously Presented) A data processor comprising:

a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising a plurality of the syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment; and

alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles, the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes.

2. (Previously Presented) The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles.

3. (Previously Presented) The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles.

4. (Previously Presented) The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles.

5. (Previously Presented) The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said execution clusters.

6. (Original) The data processor as set forth in Claim 5 wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

7. (Previously Presented) The data processor as set forth in Claim 6 wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

1) said at least one address bit associated with each of said complete instruction bundles;

2) at least one address bit associated with at least one syllable in each of said complete instruction bundles; and

3) a cluster bit associated with each of said complete instruction bundles.

8. (Previously Presented) The data processor as set forth in Claim 1 wherein each execution pipeline is four lanes wide.

9. (Previously Presented) The data processor as set forth in Claim 1 wherein the data processor comprises three execution units.

10. (Previously Presented) A processing system comprising:

a data processor;

a memory coupled to said data processor; and

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor;

wherein said data processor comprises:

a plurality of execution clusters, each of said execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, wherein each of said instruction execution pipelines is a plurality of lanes wide, each of said lanes capable of receiving one or more of said syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising a plurality of the syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment; and

alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters as a function of at least one address bit associated with each of said complete instruction bundles, the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes.

11. (Previously Presented) The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles.

12. (Previously Presented) The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles.

13. (Previously Presented) The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in each of said complete instruction bundles.

14. (Previously Presented) The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said execution clusters.

15. (Original) The processing system as set forth in Claim 14 wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

16. (Previously Presented) The processing system as set forth in Claim 15 wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

1) said at least one address bit associated with each of said complete instruction bundles;

2) at least one address bit associated with at least one syllable in each of said complete instruction bundles; and

3) a cluster bit associated with each of said complete instruction bundles.

17. (Previously Presented) The processing system as set forth in Claim 10 wherein each execution pipeline is four lanes wide.

18. (Previously Presented) The processing system as set forth in Claim 10 wherein the data processor comprises three execution units.

19. (Previously Presented) For use in a data processor comprising a plurality of execution clusters, each of the execution clusters comprising an instruction execution pipeline having a plurality of processing stages capable of executing instruction bundles each comprising one or more syllables, wherein each of the instruction execution pipelines is a plurality of lanes wide, each of the lanes capable of receiving one or more of the syllables of the instruction bundles, a method of routing instruction bundles into the lanes in the execution clusters comprising the steps of:

fetching cache lines from an instruction cache, each of the cache lines comprising a plurality of the syllables;

issuing complete instruction bundles toward the execution clusters, wherein at least one complete instruction bundle is issued having an out-of-order alignment;

reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes; and

routing each of the complete instruction bundles to a correct one of the execution clusters as a function of at least one of:

1) at least one address bit associated with each of the complete instruction bundles;

2) at least one address bit associated with at least one syllable in each of the complete instruction bundles; and

3) a cluster bit associated with each of the complete instruction bundles.

20. (Previously Presented) The method as set forth in Claim 19 wherein each execution pipeline is four lanes wide and the data processor comprises three execution units.

21. (Previously Presented) The data processor as set forth in Claim 1, wherein each of

the execution clusters comprises one or more arithmetic units, a register file, an interface to a memory controller, and an inter-cluster communication interface.

22. (Previously Presented) The processing system as set forth in Claim 10, wherein each of the execution clusters comprises one or more arithmetic units, a register file, an interface to a memory controller, and an inter-cluster communication interface.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX B -
Copy of Formal Drawings

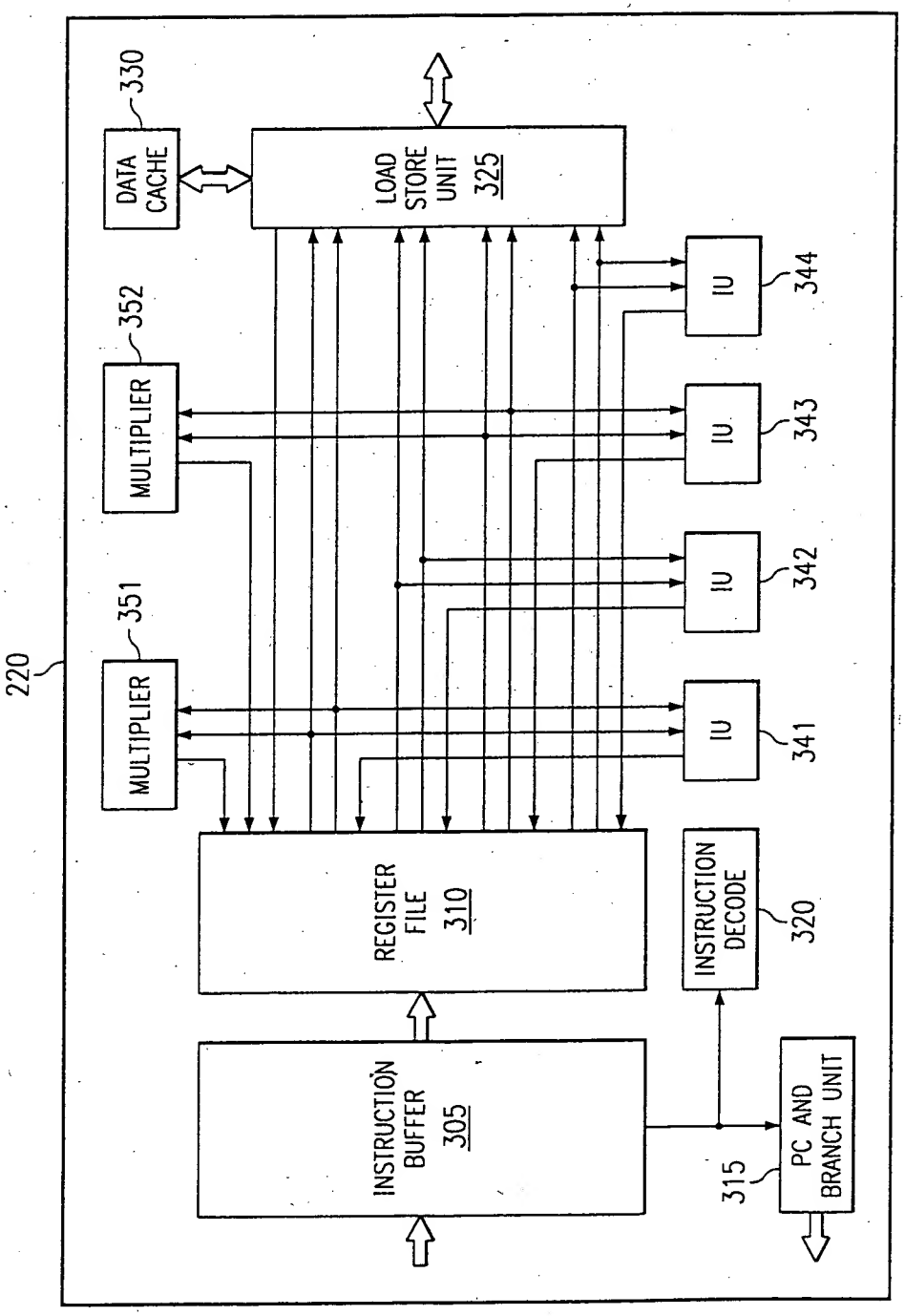

FIG. 3

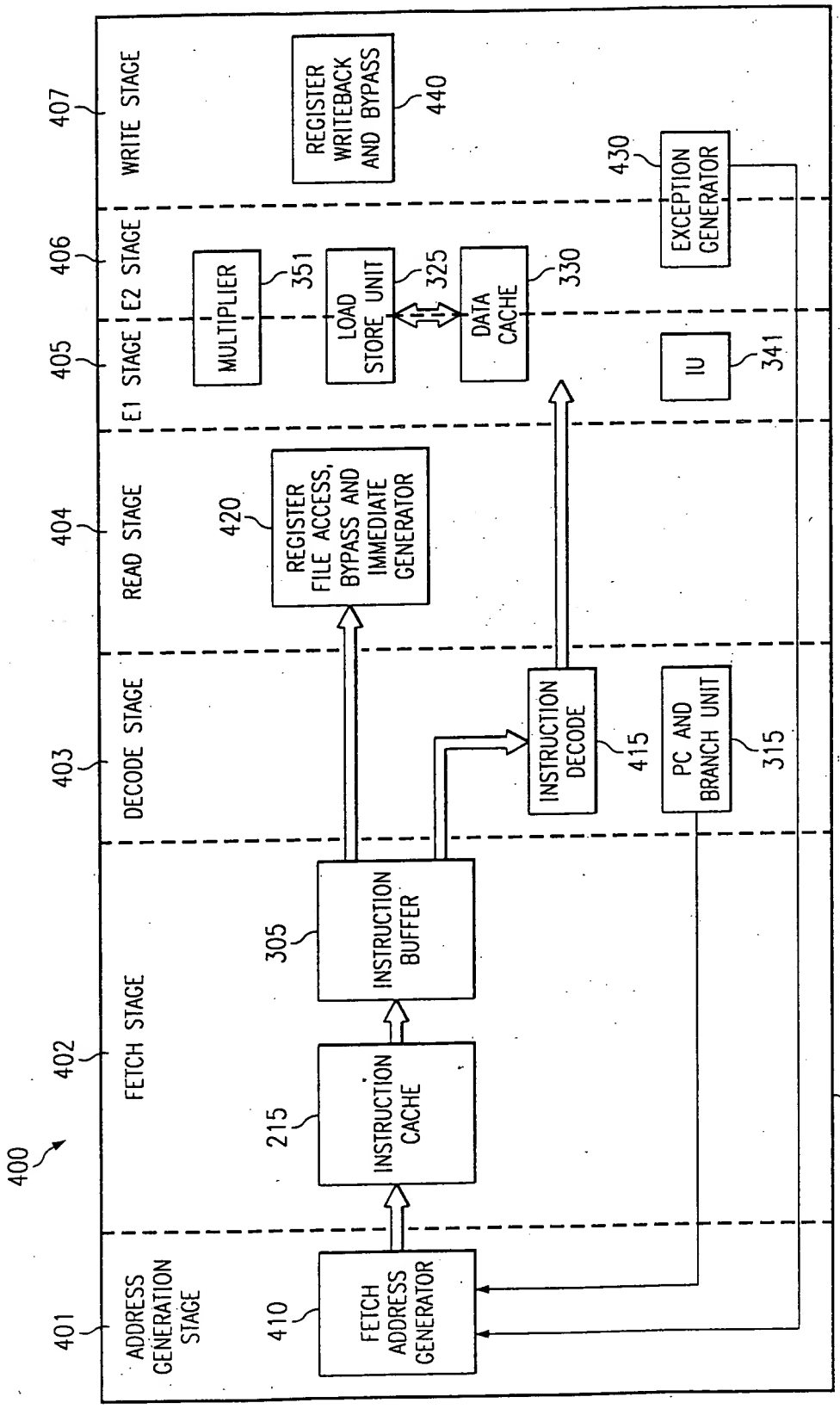

FIG. 4

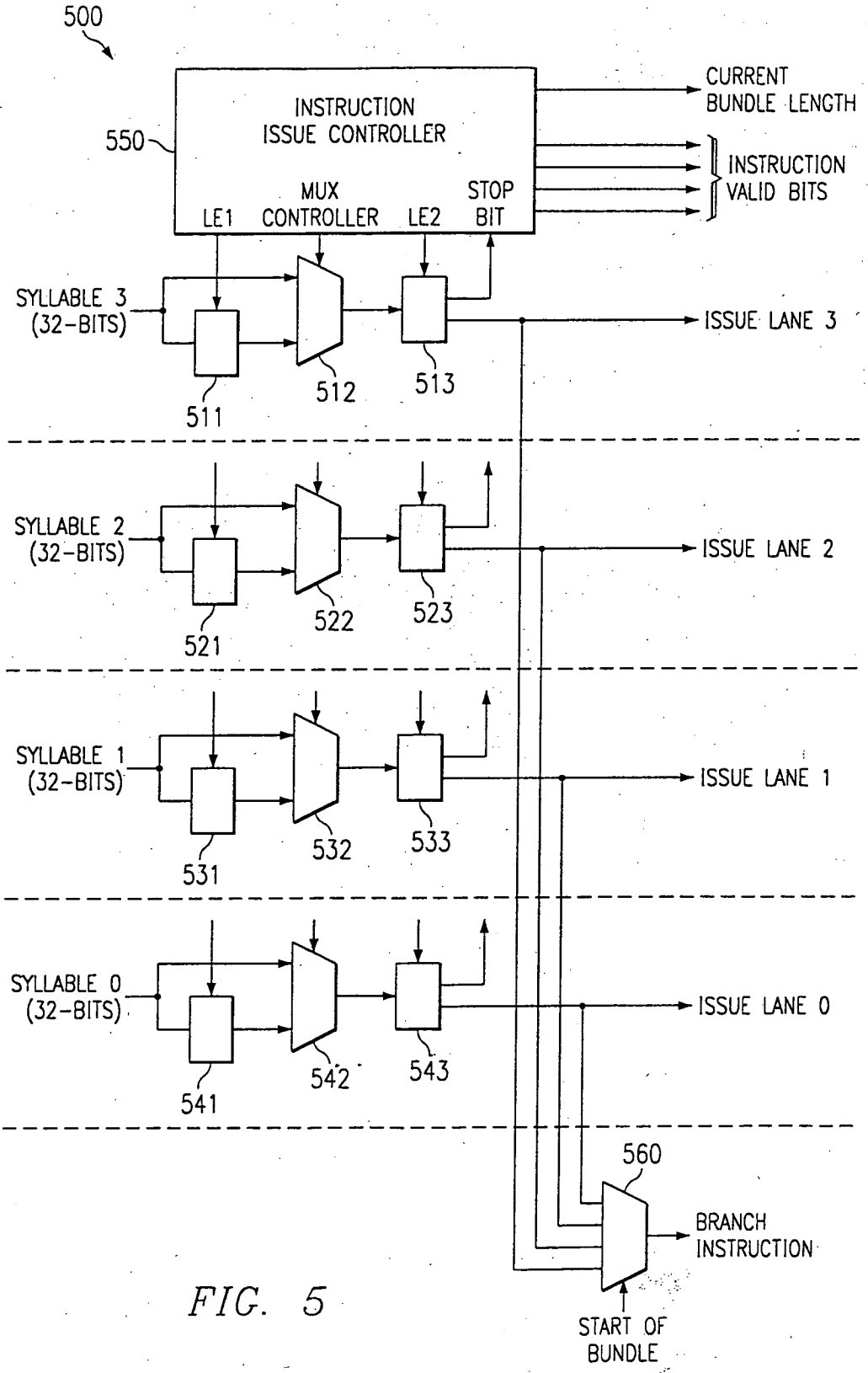

FIG. 5

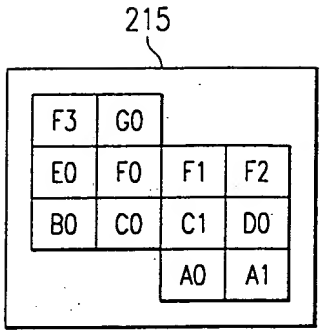

FIG. 6

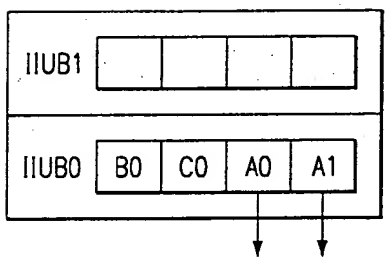

FIG. 7A

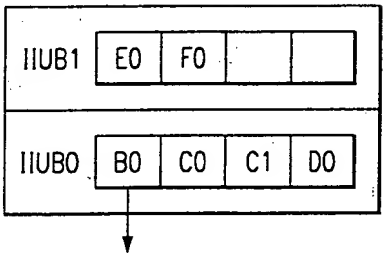

FIG. 7B

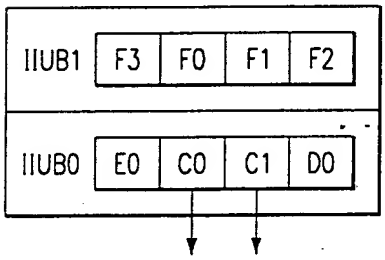

FIG. 7C

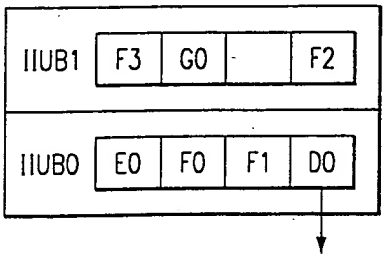

FIG. 7D

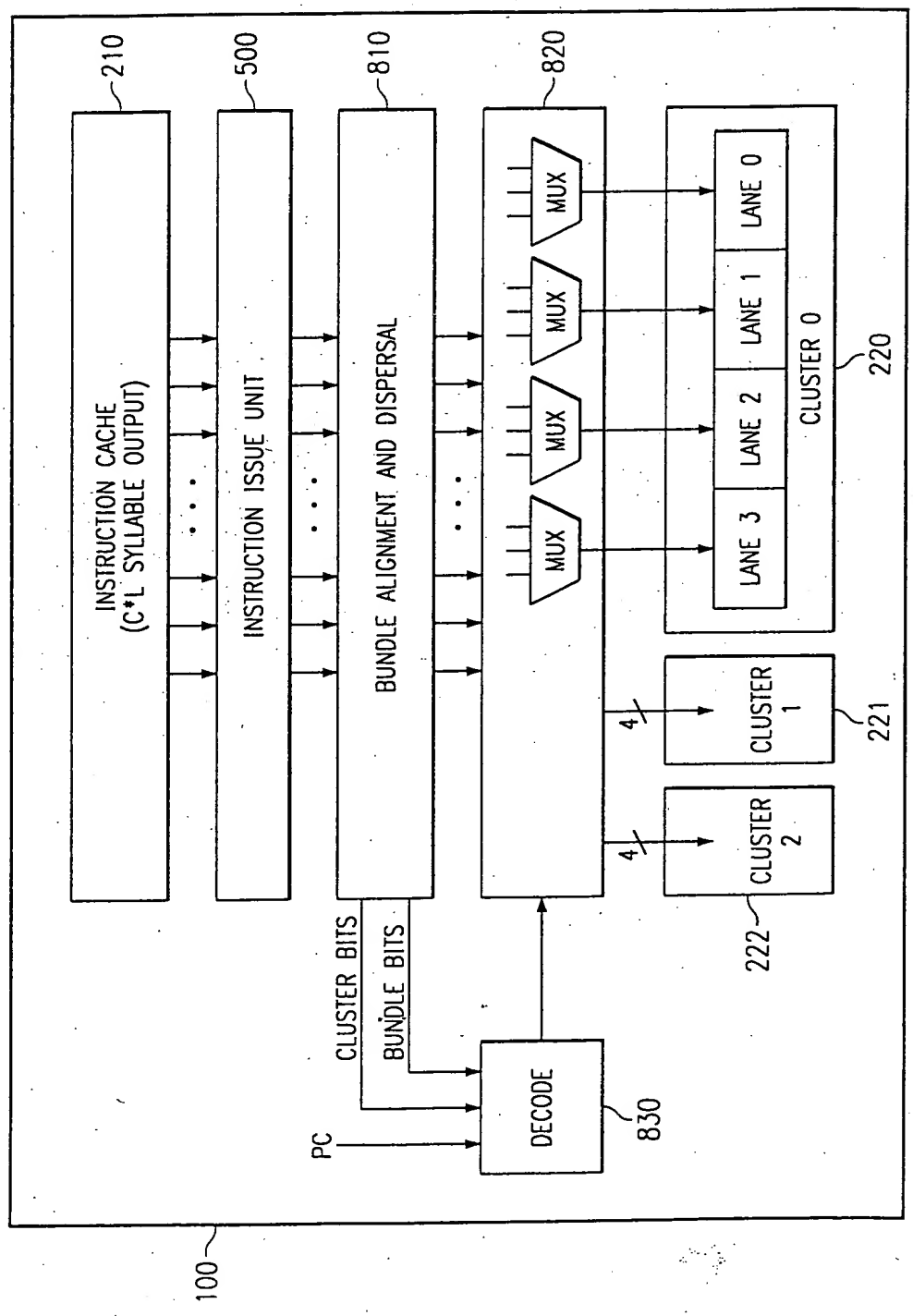

FIG. 8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX C -

Evidence Appendix

None.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Paolo Faraboschi, et al.
Serial No.:	09/751,674
Filed:	December 29, 2000
For:	CIRCUIT AND METHOD FOR INSTRUCTION COMPRESSION AND DISPERSAL IN WIDE-ISSUE PROCESSORS
Group No.:	2183
Examiner:	Aimee J. Li

APPENDIX D -
Related Proceedings Appendix

Not Applicable – To the best knowledge and belief of the undersigned attorney, there are none.